REMARKS

Claims 1-8 and 10-21 are pending and at issue. Claims 1-4, 6-8, 11-17 stand rejected as anticipated by Flautner (U.S. Patent No. 7,134,031). The remaining claims each stand rejected under a proposed combination of Flautner and Choi et al. et al. (U.S. Patebt No. 6,233,690). Claim 9 is canceled. In light of the following remarks, Applicant respectfully asserts that the relied upon art does not teach or suggest the recited subject matter. Reconsideration of the rejection in light of the same is therefore respectfully requested.

Claims 1 and 13 are amended to recite obtaining data on runtime performance of a thread that is indicative of a set of execution characteristics of the thread including an instructions per clock cycle metric. This amendment is supported by the specification at least at paragraph 0028.

Applicant respectfully traverses the rejection of claims 1-4, 6-8, 11-17 as anticipated by Flautner. Each of the pending claims recites obtaining thread runtime performance data that is indicative of a set of execution characteristics of a thread including an instructions per clock cycle metric. The pending claims further recite adjusting an operating voltage or an operating frequency of the machine based on the performance data. Flautner does not disclose obtaining thread runtime performance data that is indicative of a set of execution characteristics and that includes an instructions per clock cycle metric. Therefore, Flautner does anticipate claims 1-4, 6-8, 11-17.

While Flautner discloses reducing power to a set of processors based on a degree of thread level parallelism between two or more processors, Flautner does not disclose measuring or obtaining an instructions per clock cycle metric. Flautner defines parallelism as a "measure [of] how many parallel threads, which may be from independent processes or from a single process, are executing in parallel for periods when at least one such thread is executing." (Col. 2, lines 62-65). That is, Flautner's system merely discusses measuring how many threads are active (or actually executing instructions) at the same time, which is entirely different from measuring how many instructions are being executed by a thread during a period of time (e.g., a clock cycle). In fact, parallelism, as defined by Flautner, does not provide a measure of rate, in any manner. As Flautner does not disclose obtaining thread runtime performance data that is indicative of a set of execution characteristics that includes an instructions per clock cycle metric, Flautner does not anticipate claims 1-4, 6-8, and 11-17.

Moreover, Flautner does not suggest or teach adjusting an operating voltage or an operating frequency of the machine based on an instructions per cycle metric, as recited by the pending claims. Instead, the system of Flautner adjusts its operating voltage and frequency by determining when two or more threads or processors are in an active state (i.e., executing instructions in parallel). As long as a thread is processing some instructions (at least one instruction), the thread is considered active. The number of threads, however, is not indicative of the number of instructions being executed per cycle. Thus, Flautner does not consider an instruction rate, such as the recited instructions per cycle metric, as relevant in its parallelism determination. Accordingly, Flautner does not suggest or teach adjusting an operating voltage or an operating frequency based on an instructions per cycle metric.

Applicant respectfully traverses the rejection of claims 7 and 19-20 as obvious over Flautner. Each of the claims recites obtaining thread runtime performance data that is indicative of a set of execution characteristics of a thread including an instructions per clock cycle metric. As discussed above, Flautner does not disclose or teach measuring an instructions per clock cycle metric, and thus, Flautner does not render claims 7 and 19-20 obvious.

Applicant respectfully traverses the rejection of claims 5, 9-10, 18 and 21 as obvious in view of Flautner and Choi et al. (U.S. Patent No. 6,233,690). Each of the pending claims recites obtaining thread runtime performance data that is indicative of a set of execution characteristics of a thread including an instructions per clock cycle metric, and adjusting an operating voltage or an operating frequency of the machine based on the performance data. Neither Flautner nor Choi et al. discloses thread runtime performance data that is indicative of a set of execution characteristics of a thread that includes an instructions per clock cycle metric. Therefore, no combination of Flautner and Choi et al. can render any of the pending claims obvious.

As discussed above, Flautner does not disclose or teach an instructions per clock cycle metric. While Choi et al. discloses detecting the presence of incoming instructions to wake a processor, Choi et al. also does not disclose measuring an instructions per cycle metric. Specifically with respect to canceled claim 9, the Office action cites Choi et al. at Col. 1, lines 40-45 for disclosing an instructions per cycle metric:

> The clock signal is restored to the affected components when an input is detected. At a finer level of control, execution logic within the processor may be decoupled from the clock if it does

> not detect any incoming instructions to be processed. The execution logic is powered up when an appropriate instruction is detected in the processor pipeline. Col. 1, lines 40-45.

At best, this passage teaches determining when at least one instruction is present or available. The availability of a single instruction does not indicate a count of the number of instructions available. Moreover, the presence or availability of a single instruction is not indicative of a rate of instructions, such as an instruction per cycle metric. In particular, a rate is a count over a period, and thus, the instructions per cycle metric is a number of instructions (e.g., being executed by the processor) over a single clock cycle. Choi et al. fails to disclose any instruction count over any period of time.

Moreover, Choi et al., similar to Flautner, fails to suggest or teach measuring a number of instructions per period of time. Generally, the Choi system determines before the execution of an instruction whether data needed for the instruction is available, and if it is not, the Choi system may turn off the processor until the data is available:

> The cache unit monitors a load operation and generates a data return signal in advance of the load return. The hazard unit tracks data status and generates a stall signal when data required by an instruction is not available. The gating module adjusts power to the execution unit according to the state of the data return and stall signals. Col. 2, lines 19-25.

> Power adjustments are accomplished by gating a clock signal to targeted logic. Here, gating refers to decoupling the clock signal from the targeted logic to power down the logic.... Col. 2, line 66 – Col. 3, line1.

Regardless of how many instructions the Choi et al. processor is executing for a given period, the Choi et al. processor will operate to turn off its processor when an instruction is encountered that requires data that is unavailable. Thus, Choi et al. operates to turn off its processor regardless of the number of instructions being processed and does not otherwise suggest or teach an instructions per cycle metric, as recited by the pending claims.

Because neither Flautner nor Choi et al. discloses the recited instructions per clock cycle metric, no combination of Flautner and Choi et al. can render any of pending claims 5, 9-10, 18 and 21 obvious.

CONCLUSION

For the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections/objections and allowance of claims 1-8 and 10-21.

While no fees are believed to be due with this response, the Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

If there are matters that can be discussed by telephone to further the prosecution of this application, Applicant respectfully requests that the Examiner call its attorney at the number listed below.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: August 30, 2007

Respectfully submitted,

By 

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